**Lab 2 Report Hardik J Patel**

**EEC 180B 999121498**

**Combinational Logic Design using Verilog**

**Objective**

The purpose of this lab was to use Verilog to design combinational arithmetic circuits and using testbenches to verify the circuits on ModelSim. This lab also introduces us to self-checking testbenches.

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**Design and Test Procedure**

Part 1: For this part, using the given equations for a full adder, a **Behavioral** model for the full adder was implemented in Verilog, on the Quartus II software. The full bit adder was instantiated 8 times build an 8 bit ripple carry adder. The adder also included implementations in case of an Overflow. Lastly, the test bench written during the pre-lab was modified to simulate the 8 bit ripple carry adder. The three documents have been attached to the report at the end.

Part 2: In this part, a structural model of the given Array Multiplier Circuit Block Diagram was used to create a **Structural** model of the multiplier and the multiplier was tested on the DE2 board. The performance of the circuit was then estimated in terms of the critical path using the timing analysis tool.

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**Conclusion**

This lab taught us the implementation of self-checking test benches as well as behavioral and structural models in verilog.

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_